WHAT IS CLAIMED IS:

1. An impedance trimming circuit comprising:

a common bias section composed of a first series circuit having a first internal resistor and an external resistor connected in series via a first node and a first operational amplifier having a first input terminal connected to an internal reference voltage, a second input terminal connected to the first node, and an output terminal connected to the first series circuit; and

an impedance trimming section composed of a second series circuit having a second internal resistor and an impedance dummy resistor connected in series via a second node, a comparator having a first input terminal connected to the first node and a second input terminal connected to the second node, a code control circuit which uses a clock signal to latch an output signal from the comparator to generate a plurality of switching codes, and a switching circuit which uses the plurality of switching codes to switch a resistance value of the impedance dummy resistor,

wherein the first operational amplifier is also connected to the second series circuit, and an output signal from the code control circuit is inputted to a target impedance trimming circuit.

2. The impedance timing circuit according to claim 1, wherein one or more pairs of the common bias

section and the impedance trimming section are present.

3. The impedance timing circuit according to claim 1, wherein the impedance dummy resistor includes an output buffer.

4. The impedance timing circuit according to claim 1, wherein the impedance dummy resistor includes input impedance, terminal resistance, and pull-up resistance or pull-down resistance.

5. The impedance timing circuit according to claim 1, wherein the plurality of switching codes from the switching circuit and a resistance value of the impedance dummy resistor exhibit a reciprocal relationship, a polygonal-line relationship, or an S-shaped relationship.

6. The impedance timing circuit according to claim 1, wherein resistance values for the first and second internal resistors contain parasitic resistance parasitic on a package, a lead, or a frame, and are adjusted to shift an adjustment range of the resistance value of the impedance dummy resistor.

7. The impedance timing circuit according to claim 1, wherein the external resistor is an external accurate resistor, and the resistance values for the first and second internal resistors can be switched on the basis of a value for the external resistor.

8. The impedance timing circuit according to claim 1, wherein the resistance values for the first

and second internal resistors are switched on the basis of the parasitic resistance parasitic on the package, lead, and frame, as well as the value for the external resistor.

9. The impedance timing circuit according to claim 1, wherein the first internal resistor is composed of a first and second resistance elements, the first resistor generates a voltage equal to a difference between a value for the internal reference value during design and a value for the internal reference value during operation, and reference values of the first and second resistance elements are adjusted in accordance with the value for the internal reference value so as to meet the following relationship:

Rext : R1under + R1upper = Rtrim : Rt

(where Rext denotes the resistance value of the external resistor, R1under denotes the resistance value of the first resistance element, R1upper denotes the resistance value of the second resistance element, Rtrim denotes the resistance value of the impedance dummy resistor, and Rt denotes a resistance value of the second internal resistor).

10. The impedance timing circuit according to claim 1, wherein the external resistor is replaced with an internal resistor which operates more accurately than the first and second internal resistors and

impedance dummy resistor.

11. The impedance timing circuit according to claim 1, wherein the impedance trimming section has a second operational amplifier, a first input terminal of the second operational amplifier is connected to the first series circuit, and a second input terminal and an output terminal of the second operational amplifier are connected to the second series circuit.